# Load Switch ICs for Portable Equipment 

## BD6528HFV,BD6529GUL

## - Description

Power switch for memory card Slot (BD6528HFV, BD6529GUL) is a high side switch IC having one circuit of N -channel Power MOSFET. This switch IC achieves ON resistance of $100 \mathrm{~m} \Omega$ with BD6529GUL; and $110 \mathrm{~m} \Omega$ with BD6528HFV. Operations from low input voltage (VIN $\leqq 2.7 \mathrm{~V}$ ) is possible; made for use of various switch applications. BD6524HFV is available in a space-saving HVSOF6 package. BD6529GUL is available in a space-saving VCSP-6 package.

## - Features

1) Single channel of Low On-Resistance (Typ. $=100 \mathrm{~m} \Omega$ ) N -channel MOSFET built in
2) 500 mA output current
3) Low voltage switch capability
4) Soft-start function
5) Output discharge circuit
6) Reverse current flow blocking at switch off
7) HVSOF6 package for BD6528HFV VCSP50L1 package for BD6529GUL

## -Applications

Memory card slots of Mobile phone, Digital still camera, PDA, MP3 player, PC, etc.

- Line up matrix

| Part Number | ON resistance | Output current | Discharge circuit | Logic Control Input | Package |
| :--- | :---: | :---: | :---: | :---: | :---: |
| BD6528HFV | $110 \mathrm{~m} \Omega$ | 500 mA | $O$ | High | HVSOF6 <br> $1.6 \times 3.0 \mathrm{~mm}$ |
| BD6529GUL | $100 \mathrm{~m} \Omega$ | 500 mA | $O$ | High | VCSP50L1 |
| $1.5 \times 1.0 \mathrm{~mm}$ |  |  |  |  |  |

- Absolute maximum ratings

| Parameter | Symbol | Ratings | Unit |
| :--- | :---: | :---: | :---: |
| Supply voltage | VDD | $-0.3 \sim 6.0$ | V |
| VIN voltage | VIN | $-0.3 \sim 6.0$ | V |
| EN voltage | VEN | $-0.3 \sim$ VDD +0.3 | V |
| VOUT voltage | VouT | $-0.3 \sim 6.0$ | V |
| Storage temperature | TSTG | $-55 \sim 150$ | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | Pd | 849 *1 (BD6528HFV) | mW |
|  |  | $575 * 2($ BD6529GUL) |  |

*1 Mounted on 70 mm * 70 mm * 1.6 mm Glass-epoxy PCB. Derating: $6.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$
*2 Mounted on 50 mm * 58 mm * 1.75 mm Glass-epoxy PCB. Derating: $4.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ at $\mathrm{Ta}>25^{\circ} \mathrm{C}$

* This product is not designed for protection against radioactive rays.
* Operation is not guaranteed.


## - Operating conditions

| Parameter | Symbol | Ratings |  |  | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |
| Operating voltage | VDD | 2.7 | 3.3 | 4.5 | V |
| Switch input voltage | VIN | 0 | 1.2 | 2.7 | V |
| Operation temperature | TOPR | -25 | 25 | 85 | ${ }^{\circ} \mathrm{C}$ |
| Output current | ILO | 0 | - | 500 | mA |

## - Electrical characteristics

OBD6528HFV(unless otherwise specified, $\mathrm{VDD}=3.3 \mathrm{~V}, \mathrm{VIN}=1.2 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Limits |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| [Current consumption] |  |  |  |  |  |  |
| Operating current | IDD | - | 20 | 30 | $\mu \mathrm{A}$ | $\mathrm{VEN}=1.2 \mathrm{~V}$ |
| Standby current | Istb | - | 0.01 | 1 | $\mu \mathrm{A}$ | $\mathrm{VEN}=0 \mathrm{~V}$ |
| [1/O] |  |  |  |  |  |  |
| EN input voltage | Venh | 1.2 | - | - | V | High level input |
|  | Venl | - | - | 0.4 | V | Low level input |
| EN input current | IEN | -1 | - | 1 | $\mu \mathrm{A}$ | $\mathrm{VEN}=0 \mathrm{~V}$ or $\mathrm{VEN}=1.2 \mathrm{~V}$ |
| [Power switch] |  |  |  |  |  |  |
| On-resistance | Ron | - | 110 | - | $\mathrm{m} \Omega$ | IOUT $=500 \mathrm{~mA}$ |
| Switch leakage current | ILEAK | - | 0.01 | 10 | $\mu \mathrm{A}$ | VEN $=0 \mathrm{~V}$, Vout $=0 \mathrm{~V}$ |
| Output rise time | Ton1 | - | 0.5 | 1 | ms | RL $=10 \Omega$, Vout $10 \% \rightarrow 90 \%$ |
| Output turn-on time | Ton2 | - | 0.6 | 2 | ms | RL $=10 \Omega$, VEn High $\rightarrow$ Vout 90\% |
| Output fall time | Toff1 | - | 1 | 20 | $\mu \mathrm{s}$ | RL $=10 \Omega$, Vout $90 \% \rightarrow 10 \%$ |
| Output turn-off time | Toff2 | - | 15 | 100 | $\mu \mathrm{s}$ | RL = 10ת, VEN Low $\rightarrow$ Vout 10\% |
| [Discharge circuit] |  |  |  |  |  |  |
| Discharge on-resistance | Rdisc | - | 70 | 110 | $\Omega$ | Iout $=-1 \mathrm{~mA}, \mathrm{VEN}=0 \mathrm{~V}$ |
| Parameter | Idisc | - | 15 | 20 | mA | Vout $=3.3 \mathrm{~V}, \mathrm{VEN}=0 \mathrm{~V}$ |

OBD6529GUL(unless otherwise specified, $\mathrm{VDD}=3.3 \mathrm{~V}, \mathrm{VIN}=1.2 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Limits |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| [Current consumption] |  |  |  |  |  |  |
| Operating current | IdD | - | 20 | 30 | $\mu \mathrm{A}$ | $\mathrm{VEN}=1.2 \mathrm{~V}$ |
| Standby current | Іstb | - | 0.01 | 1 | $\mu \mathrm{A}$ | $\mathrm{VEN}=0 \mathrm{~V}$ |
| [I/O] |  |  |  |  |  |  |
| EN input voltage | Venh | 1.2 | - | - | V | High level input |
|  | Venl | - | - | 0.4 | V | Low level input |
| EN input current | IEN | -1 | - | 1 | $\mu \mathrm{A}$ | $\mathrm{VEN}=0 \mathrm{~V}$ or V EN $=1.2 \mathrm{~V}$ |
| [Power switch] |  |  |  |  |  |  |
| On Resistance | Ron | - | 100 | - | $\mathrm{m} \Omega$ | Iout $=500 \mathrm{~mA}$ |
| Switch leakage current | ILEAK | - | 0.01 | 10 | $\mu \mathrm{A}$ | VEN $=0 \mathrm{~V}$, Vout $=0 \mathrm{~V}$ |
| Output turn on rise time | ToN1 | - | 0.5 | 1 | ms | RL $=10 \Omega$, Vout $10 \% \rightarrow 90 \%$ |
| Output turn on time | ToN2 | - | 0.6 | 2 | ms | RL $=10 \Omega$, VEN High $\rightarrow$ Vout 90\% |
| Output turn off fall time | Toff1 | - | 0.1 | 4 | $\mu \mathrm{s}$ | RL $=10 \Omega$, Vout $90 \% \rightarrow 10 \%$ |
| Output turn off time | Toff2 | - | 1 | 6 | $\mu \mathrm{s}$ | RL = 10ת, VEN Low $\rightarrow$ Vout 10\% |
| [Discharge circuit] |  |  |  |  |  |  |
| Discharge on-resistance | Rdisc | - | 70 | 110 | $\Omega$ | IOUT $=-1 \mathrm{~mA}, \mathrm{VEN}=0 \mathrm{~V}$ |
| Discharge current | IdIsc | - | 15 | 20 | mA | Vout $=3.3 \mathrm{~V}, \mathrm{VEN}=0 \mathrm{~V}$ |

- Test circuit


Fig. 1 Measurement circuit

## -Switch output turn ON/OFF timing



Fig. 2 Timing diagrams

## - Reference data



Fig. 3 Operating current EN enable


Fig. 6 Standby current EN disable


Fig. 9 On-resistance vs. VDD (BD6528HFV)


Fig. 12 On-resistance vs. IOUT (BD6528HFV)


Fig. 4 Operating current EN enable


Fig. 7 EN input voltage


Fig. 10 On-resistance vs. temperature (BD6528HFV)


Fig. 13 On-resistance vs. VDD (BD6529GUL)


Fig. 5 Standby current EN disable


Fig. 8 EN input voltage


Fig. 11 On-resistance vs. VIN (BD6528HFV)


Fig. 14 On-resistance vs. temperature (BD6529GUL)


Fig. 15 On-resistance vs. VIN (BD6529GUL)


Fig. 18 Output rise time


Fig. 21 Output fall time


Fig. 24 Output turn-off time


Fig. 16 On-resistance vs. Iout
(BD6529GUL)


Fig. 19 Output turn-on time


Fig. 22 Output fall time


Fig. 25 Discharge on-resistance


Fig. 17 Output rise time


Fig. 20 Output turn-on time


Fig. 23 Output turn-off time


Fig. 26 Discharge on-resistance

## - Waveform data



Fig. 27 Output turn-on response BD6528HFV


Fig. 29 Output turn-on response BD6528HFV


Fig. 31 Output turn-on response
BD6529GUL


Fig. 33 Output turn-on response BD6529GUL


Fig. 28 Output turn-off response BD6528HFV


Fig. 30 Output turn-off response BD6528HFV


Fig. 32 Output turn-off response BD6529GUL


Fig. 34 Output turn-off response BD6529GUL


Fig. 35 Rush current response

## - Block diagram



Fig. 36 Block diagram

| B | VIN | VOUT | VOUT |
| :---: | :---: | :---: | :---: |
| $A$ | VDD | EN | GND |
|  | 1 | 2 |  |

BD6529GUL (Bottom view)


BD6528HFV (Top view)

Fig. 37 Pin configuration

## -Pin description

| Pin number | Pin name | Pin function |
| :---: | :---: | :--- |
| 1 <br> (A3) | GND | Ground |
| 2,3 <br> (B2, B3) | VOUT | Switch output <br> (connect each pin externally) |
| 4 <br> (B1) | VIN | Switch input |
| 5 <br> (A1) | VDD | Power supply <br> (for switch control and drive circuit) |
| 6 <br> (A2) | EN | Enable input <br> (Active-High Switch on input) |

- I/O equivalent circuit

| Pin name | Pin number | Equivalent circuit |
| :---: | :---: | :---: |
| EN | $\begin{gathered} 6 \\ (\mathrm{~A} 2) \end{gathered}$ |  |
| VIN <br> VOUT | $\begin{gathered} 4 \\ (\mathrm{~B} 1) \\ 2,3 \\ (\mathrm{~B} 2, \mathrm{~B} 3) \end{gathered}$ |  |

## -Operation description

## 1. Switch operation

Each VIN and VOUT pins are connected to MOSFET's drain and source. By setting EN input to High level, the internal charge pump operates and turns on MOSFET.
When MOSFET is turned on, the switch becomes bidirectional characteristics. Consequently, in case of VIN < VOUT, the current is flowing from VOUT to VIN.
Since there is no parasitic diode between switch's drain and source, it prevents the reverse current flow from VOUT to VIN during switch off stage.
2. Output discharge circuit

Discharge circuit operates when switch is off. When discharge circuit operates, $70 \Omega$ (Typ.) resistor is connected between VOUT pin and GND pin. This discharges the electrical charge quickly.


Fig. 38 Operation timing

## - Application circuit example



Fig. 39 Application circuit example

* This application circuit does not guarantee its operation.

When the external circuit constant, etc. is changed, be sure to consider adequate margins; by taking into account external parts and/or IC's dispersion including not only static characteristics, but also transient characteristics.

## -Power dissipation characteristics



Fig. 40 Power dissipation curve (Pd-Ta Curve)
(HVSOF6 package)


Fig. 41 Power dissipation curve (Pd-Ta Curve) (VCSP50L1 package)

## - Notes foe use

## (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.
(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.
(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
(5) Operation in strong electromagnetic field Be noted that using ICs in the strong electromagnetic field can malfunction them.
(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.
(8) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (PD) in actual states of use.

## -Ordering part number



Part No.


Part No.
6528
6529

-


Packaging and forming specification
TR: Embossed tape and reel (HVSOF6)
E2: Embossed tape and reel (VCSP50L1)

## HVSOF6


<Tape and Reel information>

| Tape | Embossed carrier tape |
| :--- | :--- |
| Quantity | 3000 pcs |
| Direction <br> of feed | TR <br> $\left(\begin{array}{l}\text { The direction is the 1pin of product is at the upper right when you hold } \\ \text { reel on the left hand and you pull out the tape on the right hand }\end{array}\right.$ |



## VCSP50L1(BD6529GUL)




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